CS4223: Multi-Core Architectures

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**Cache simulator**

**Language** : C++

**Implementation**

**-Basic CPU**

CPU class, which have cpu id, cache, bus, dram, cycles, etc..

**-Read line(from data files)**

Read label and data. Input of cpu execution

**-Cache access (if fail, mem access)**

Request data to cache if not, target cycles change for mem access

**-Bus access**

Not implemented yet.

**-Compute cycles**

Add cycles for an instruction to total cycles

**Input example**

Just “make” then “./coherence MESI blackscholes\_ 1024 1 16”

텍스트, 전자제품, 디스플레이, 디스플레이 장치이(가) 표시된 사진

자동 생성된 설명

**Output**

- Overall cycles

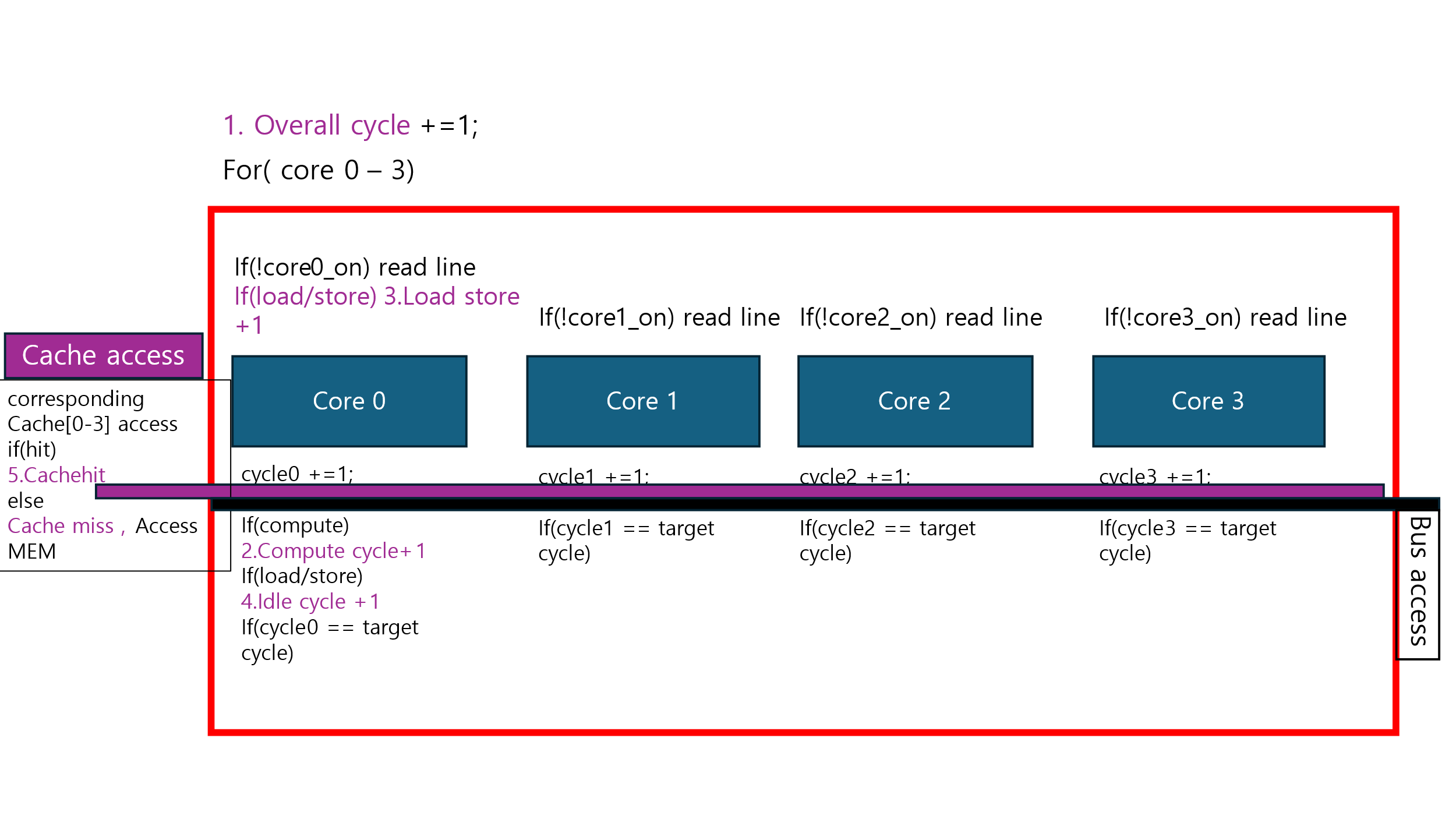
- Compute cycles

- # of Load/store

- Idle cycles

- Cache hit / miss

**Process**



But we only implemented Single Core yet.

**Cycles datail**

